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REMARKS

By the present amendment and response, independent claims 1, 10, 14, 18, and 26 have been amended to overcome the Examiner's objections and claims 2-5 have been canceled. Thus, claims 1, 6-10, 14-18, 20-24, 26, 28-31, and 33-36 remain in the present application and claims 33-36 have been allowed. Reconsideration and allowance of outstanding claims 1, 6-10, 14-18, 20-24, 26, and 28-31 in view of the following remarks are requested.

In the ***final rejection*** of January 2, 2004, the Examiner has rejected claims 10, 14, 26, 28, and 31 under 35 USC §103(a) as being unpatentable over U.S. patent number 6,245,682 to Fu et al. ("Fu"), U.S. patent number 5,597,754 to Lou et al. ("Lou"), and "Silicon Processing for the VLSI Era Volume 1: Process Technology," pp. 429-455 and 518, by Wolf et al. ("Wolf"). For the reasons discussed below, Applicant respectfully submits that the present invention, as defined by amended independent claims 10, 14, and 26, is patentably distinguishable over Fu, Lou, and Wolf, singly or in any combination thereof.

The present invention, as defined by amended independent claim 10, teaches, among other things, "etching the remaining layer of silicon oxynitride in the stack in a phosphoric acid etchant without subjecting the layer of silicon oxynitride to any temperature greater than about 400°C after the step of depositing the layer of silicon oxynitride," "forming a layer of oxide on the edge of the stack after the step of etching the remaining layer of silicon oxynitride in the stack." As disclosed in the present application, the layer of silicon oxynitride remaining in the stack must be removed

without causing serious etching of the exposed edges of the remaining layers in the stack, such as the exposed edge of silicon nitride in an interpoly layer. To accomplish this, the silicon oxynitride can be effectively removed at a fast etch rate of about 6nm per minute in hot phosphoric acid.

However, if the silicon oxynitride has been subjected to any high temperature treatment, such as an oxidation process, the etch rate of the silicon oxynitride in the hot phosphoric acid is undesirably low, which causes serious etching of the exposed edge of the silicon nitride in the interpoly layer. Thus, by ensuring that the layer of silicon oxynitride is not subjected to a temperature greater than about 400°C after it has been depositing, the layer of silicon oxynitride in the stack can be effectively removed at sufficiently fast etch rate of about 6nm per minute utilizing the present invention.

Also, as disclosed in the present application, as a result of slight etching of the nitride layer in the interpoly dielectric layer during removal of the layer of silicon oxynitride, a notch can be formed in the exposed edge of the nitride layer. By growing an oxide layer on the layer of polycrystalline silicon and the floating gate exposed at the edges of the stack, the edges of the layer of polycrystalline silicon and the floating gate can be advantageously brought into alignment with the edge of the silicon nitride that was etched, i.e. "notched," during the removal of the layer of silicon oxynitride.

In contrast to the present invention as defined by amended independent claim 10, Fu does not teach, disclose, or suggest "etching the remaining layer of silicon oxynitride in the stack in a phosphoric acid etchant without subjecting the layer of silicon oxynitride to any temperature greater than about 400°C after the step of depositing the layer of

silicon oxynitride," "forming a layer of oxide on the edge of the stack after the step of etching the remaining layer of silicon oxynitride in the stack." Fu specifically discloses etching a stack comprising ARC layer 10, thermal oxide layer 8, and polysilicon layer 6 to define polysilicon gate feature 14. See, for example, column 4, line 67, column 5, lines 1-6, and Figures 1 and 2 of Fu. In Fu, thin protective oxide layer 16 is then formed on the sidewalls of polysilicon gate feature 14. See, for example, column 5, lines 11-13 and Figure 3 of Fu. In Fu, after thin protective oxide layer 16 has been formed on the sidewalls of polysilicon gate feature 14, ARC layer 10 is removed by means of a hot H_3PO_3 etching process. See, for example, Fu, column 5, lines 23-25.

Thus, in Fu, an oxide layer, i.e. thin protective oxide layer 16, is formed on the sidewalls of polysilicon gate feature 14, i.e. a stack, before removal of ARC layer 10. In contrast, amended independent claim 10 specifies "forming a layer of oxide on the edge of the stack after the step of etching the remaining layer of silicon oxynitride in the stack." Furthermore, in Fu, thin protective oxide layer 16 is utilized to protect the sidewall surfaces of polysilicon gate feature 14 during removal of ARC layer 10. See, for example, Fu, column 5, lines 32-35.

Thus, Fu teaches away from forming thin protective oxide layer 10 after the removal of ARC layer 10. Moreover, Fu fails to teach, disclose, or suggest etching the remaining layer of silicon oxynitride in the stack in a phosphoric acid etchant without subjecting the layer of silicon oxynitride to any temperature greater than about 400°C after the step of depositing the layer of silicon oxynitride. Additionally, Fu provides no motivation for etching ARC layer 10 in a phosphoric acid etchant without subjecting

ARC layer 10 to any temperature greater than about 400°C after the step of depositing ARC layer 10, since Fu utilizes thin protective oxide layer 16 to protect the sidewall surfaces of polysilicon gate feature 14 during removal of ARC layer 10.

In contrast to the present invention as defined by amended independent claim 10, Lou does not teach, disclose, or suggest "etching the remaining layer of silicon oxynitride in the stack in a phosphoric acid etchant without subjecting the layer of silicon oxynitride to any temperature greater than about 400°C after the step of depositing the layer of silicon oxynitride," "forming a layer of oxide on the edge of the stack after the step of etching the remaining layer of silicon oxynitride in the stack." The Examiner has cited Lou to show that thermal oxidation of polysilicon can be done at a temperature lower than 400°C.

However, as discussed above, Fu provides no motivation for etching ARC layer 10 in a phosphoric acid etchant without subjecting ARC layer 10 to any temperature greater than about 400°C after the step of depositing ARC layer 10, since Fu utilizes thin protective oxide layer 16 to protect the sidewall surfaces of polysilicon gate feature 14 during removal of ARC layer 10. Furthermore, Lou fails to teach, disclose, or suggest forming a layer of oxide on the edge of the stack after the step of etching the remaining layer of silicon oxynitride in the stack. Thus, Lou fails to cure the basic deficiencies of Fu discussed above.

In contrast to the present invention as defined by amended independent claim 10, Wolf does not teach, disclose, or suggest "etching the remaining layer of silicon oxynitride in the stack in a phosphoric acid etchant without subjecting the layer of silicon

oxynitride to any temperature greater than about 400°C after the step of depositing the layer of silicon oxynitride," "forming a layer of oxide on the edge of the stack after the step of etching the remaining layer of silicon oxynitride in the stack." The Examiner has cited Wolf to show that processing of photoresist is performed utilizing a temperature that is less than 400°C. However, Wolf in combination with Lou fail to cure the basic deficiencies of Fu discussed above.

For the foregoing reasons, Applicant respectfully submits that the present invention, as defined by amended independent claim 10, is not suggested, disclosed, or taught by Fu, Lou, and Wolf, singly or in any combination thereof. As such, the present invention, as defined by amended independent claim 10, is patentably distinguishable over Fu, Lou, and Wolf.

The present invention, as defined by amended independent claim 14, teaches, among other things, "etching the second layer in the stack in an etchant comprising hot phosphoric acid, the etching occurring before the second layer is subjected to any temperature greater than about 400°C," and oxidizing the layer of polycrystalline silicon in the stack after the step of etching the second layer in the stack." The present invention as defined by amended independent claim 14 achieves similar advantages as the present invention as defined by amended independent claim 10 discussed above. Thus, for similar reasons as discussed above, Applicant respectfully submits that the present invention, as defined by amended independent claim 14, is not suggested, disclosed, or taught by Fu, Lou, and Wolf, singly or in any combination thereof. As such, the present

invention, as defined by amended independent claim 14, is patentably distinguishable over Fu, Lou, and Wolf.

The present invention, as defined by amended independent claim 26, teaches, among other things, "removing the layer of silicon oxynitride in the stack before subjecting the layer of silicon oxynitride to a temperature greater than about 400°C after the step of depositing the layer of silicon oxynitride," and forming a layer of oxide on the edge of the stack after the step of removing the layer of silicon oxynitride in the stack. For similar reasons as discussed above, Applicant respectfully submits that the present invention, as defined by amended independent claim 26, is not suggested, disclosed, or taught by Fu, Lou, and Wolf, singly or in any combination thereof. As such, the present invention, as defined by amended independent claim 26, is patentably distinguishable over Fu, Lou, and Wolf. Thus claims 28 and 31 depending from amended independent claim 26 are, *a fortiori*, also patentably distinguishable over Fu, Lou, and Wolf for at least the reasons presented above and also for additional limitations contained in each dependent claim.

In the ***final rejection*** of January 2, 2004, the Examiner has further rejected claims 1, 6, 18, 23, and 24 under 35 USC §103(a) as being unpatentable over Fu, Lou, and Wolf, and further in view of U.S. patent number 5,620,913 to Hsiao-Lun Lee ("Lee"). For the reasons discussed below, Applicant respectfully submits that the present invention, as defined by amended independent claims 1 and 18, is patentably distinguishable over Fu, Lou, Wolf, and Lee, singly or in any combination thereof.

The present invention, as defined by amended independent claim 1, teaches, among other things, "removing the remaining layer of silicon oxynitride in the stack by etching in hot phosphoric acid before subjecting the layer of silicon oxynitride to any temperature greater than about 400°C," and "oxidizing the layer of polysilicon in the stack after the step of removing the remaining layer of silicon oxynitride in the stack." The present invention as defined by amended independent claim 1 achieves similar advantages as the present invention as defined by amended independent claim 10 discussed above. For similar reasons as discussed above, Fu, Lou, and Wolf fail to teach, disclose, or suggest "removing the remaining layer of silicon oxynitride in the stack by etching in hot phosphoric acid before subjecting the layer of silicon oxynitride to any temperature greater than about 400°C," and "oxidizing the layer of polysilicon in the stack after the step of removing the remaining layer of silicon oxynitride in the stack."

In contrast to the present invention as defined by amended independent claim 1, Lee does not teach, disclose, or suggest "removing the remaining layer of silicon oxynitride in the stack by etching in hot phosphoric acid before subjecting the layer of silicon oxynitride to any temperature greater than about 400°C," and "oxidizing the layer of polysilicon in the stack after the step of removing the remaining layer of silicon oxynitride in the stack." Lee specifically discloses the formation of stack ST2, which includes floating gate electrode polysilicon layer FG2, inter-polysilicon layer IP2, and polysilicon control gate electrode layer CG2. See, for example, Lee, column 6, lines 19-24. However, Lee fails to teach, disclose, or suggest "removing the remaining layer of silicon oxynitride in the stack by etching in hot phosphoric acid before subjecting the

layer of silicon oxynitride to any temperature greater than about 400°C," and "oxidizing the layer of polysilicon in the stack after the step of removing the remaining layer of silicon oxynitride in the stack."

For the foregoing reasons, Applicant respectfully submits that the present invention, as defined by amended independent claim 1, is not suggested, disclosed, or taught by Fu, Lou, Wolf, and Lee, singly or in any combination thereof. As such, the present invention, as defined by amended independent claim 1, is patentably distinguishable over Fu, Lou, Wolf, and Lee. Thus claim 6 depending from amended independent claim 1 is, *a fortiori*, also patentably distinguishable over Fu, Lou, Wolf, and Lee for at least the reasons presented above and also for additional limitations contained in the dependent claim.

The present invention, as defined by amended independent claim 18, teaches, among other things, "removing the layer of silicon oxynitride in the stack without subjecting the layer of silicon oxynitride to a temperature greater than about 400°C after the step of depositing the layer of silicon oxynitride," and "forming a layer of oxide on the edge of the stack after the step of removing the layer of silicon oxynitride in the stack." The present invention as defined by amended independent claim 18 achieves similar advantages as the present invention as defined by amended independent claim 10 discussed above. For similar reasons as discussed above, Fu, Lou, Wolf, and Lee, singly or in any combination thereof, fail to teach, disclose, or suggest "removing the layer of silicon oxynitride in the stack without subjecting the layer of silicon oxynitride to a temperature greater than about 400°C after the step of depositing the layer of silicon

oxynitride," and "forming a layer of oxide on the edge of the stack after the step of removing the layer of silicon oxynitride in the stack."

For the foregoing reasons, Applicant respectfully submits that the present invention, as defined by amended independent claim 18, is not suggested, disclosed, or taught by Fu, Lou, Wolf, and Lee, singly or in any combination thereof. As such, the present invention, as defined by amended independent claim 18, is patentably distinguishable over Fu, Lou, Wolf, and Lee. Thus claims 23 and 24 depending from amended independent claim 18 are, *a fortiori*, also patentably distinguishable over Fu, Lou, Wolf, and Lee for at least the reasons presented above and also for additional limitations contained in each dependent claim.

In the ***final rejection*** of January 2, 2004, the Examiner has further rejected claims 7-9, 15-17, 20-22, and 29-30 under 35 USC §103(a) as being unpatentable over Fu, Lou, Wolf, and Lee, and further in view of U.S. patent number 5,968,324 to Cheung et al. As discussed above, amended independent claim 1 is patentably distinguishable over Fu, Lou, Wolf, and Lee, amended independent claim 14 is patentably distinguishable over Fu, Lou, and Wolf, amended independent claim 18 is patentably distinguishable over Fu, Lou, Wolf, and Lee, and amended independent claim 26 is patentably distinguishable over Fu, Lou, and Wolf. As such, claims 7-9 depending from amended independent claim 1 and claim 20-22 depending from amended independent claim 18 are, *a fortiori*, also patentably distinguishable over Fu, Lou, Wolf, and Lee for at least the reasons presented above and also for additional limitations contained in each dependent claim. Also, claims 15-17 depending from amended independent claim 14 and claims 29-30

depending from amended independent claim 26 are, *a fortiori*, also patentably distinguishable over Fu, Lou, and Wolf for at least the reasons presented above and also for additional limitations contained in each dependent claim.

Based on the foregoing reasons, the present invention, as defined by amended independent claims 1, 10, 14, 18, and 26 and claims depending therefrom, is patentably distinguishable over the art cited by the Examiner. Thus, claims 1, 6-10, 14-18, 20-24, 26, and 28-31 are also patentably distinguishable over the art cited by the Examiner. For all the foregoing reasons, an early allowance of outstanding claims 1, 6-10, 14-18, 20-24, 26, and 28-31 and an early Notice of Allowance for all claims 1, 6-10, 14-18, 20-24, 26, 28-31, and 33-36 pending in the present application is respectfully requested.

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Respectfully Submitted;
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Dated: 4/30/04

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